LAKIREDDY BALI REDDY COLLEGE OF ENGINEERING (AUTONOMOUS)
Accredited by NAAC & NBA (Under Tier - I) and ISO 9001:2015 Certified Institution Approved by AICTE, New Delhi and Affiliated to JNTUK, Kakinada
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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

REPORT
on
AICTE Sponsored Online Short Term Training Program
on
"Mixed Signal Design Approaches for Artificial Intelligence Processors"
Series – 1 (28th December 2020 to 3ed January 2021)

Department of ECE of Lakireddy Bali Reddy College of Engineering (Autonomous), has organized AICTE Sponsored Online Short Term Training Program (STTP) on "**Mixed Signal Design Approaches for Artificial Intelligence Processors**" under the coordinator ship of Dr. Srinivasulu Gundala. The Program was conducted as Series - 1 of three series scheduled from **28-12-2020 to 03-01-2021.**

ABOUT AICTE – STTP:

All India Council for Technical Education (AICTE) was set up in November 1945 as a national-level apex advisory body to conduct a survey on the facilities available for technical education and to promote development in the country in a coordinated and integrated manner. And to ensure the same, as stipulated in the National Policy of Education (1986), AICTE was vested with: Short Term Training Program (STTP) intends to conduct faculty trainings through financial assistance from AICTE to enable faculty members in the field of technical education to introspect and learn techniques that can help prepare students for active and successful participants in a knowledge society.

OBJECTIVES of STTP:

The objectives of the training program:

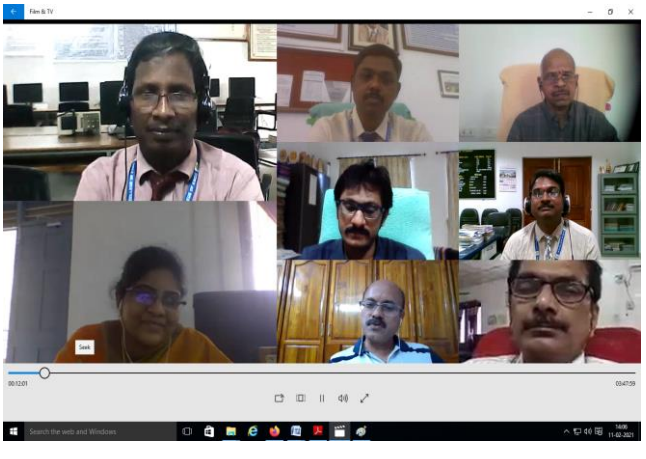
- To alleviate the Design and analysis of CMOS Mixed signal Circuits like current sources, Current and Voltage reference circuits, Voltage converters, and Data Converters of AI Processors,
- To design issues allied with high performance Mixed Signal designs.
- To provides platform to enhance the skills towards Design and development of intelligent computational systems for the Teaching faculty.

Date: 28th December 2020

Inauguration:

STTP was inaugurated on 28th December 2020 at 9:30 AM by **Dr. Y. Amar Babu** HOD of ECE and Convener of STTP along with chief guest of the programme **Dr. P Srihari Rao,** Associate Professor, NITW, Warangal, Principal of LBRCE **Dr. K. Appa Rao**, and Coordinator of STTP **Dr. Srinivasulu Gundala.**

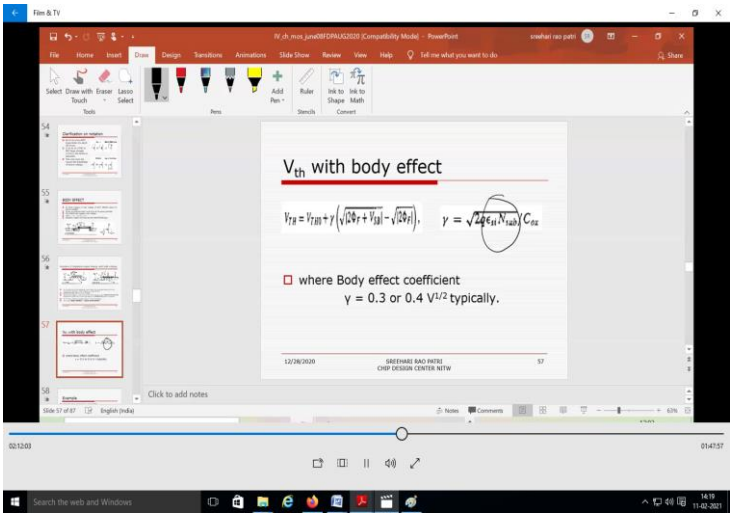
Dr. Srinivasulu Gundala, has welcomed all the delegates and participants to the STTP. In his speech, he highlighted the main objectives and importance of this Short-Term Training Programme. Along with this, he gave a brief introduction about how the selection process has done.

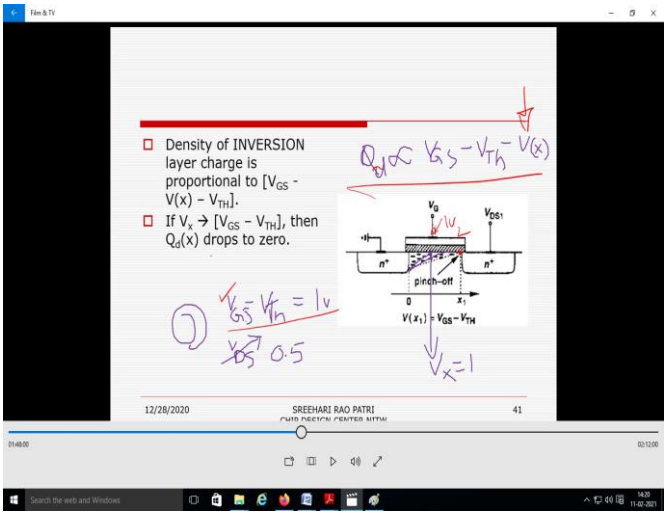


Day 1: 28th Dec 2020 [FN]

Topic : Basic building blocks, Current mirror and Differential amplifiers
Resource Person : Dr. P Srihari Rao, Associate Professor, NITW, Warangal

The resource Person **Dr. P Srihari Rao,** Associate Professor, NITW, Warangal, started his lecture by giving analysis of different design techniques for ultra low-voltage Integrated Circuits (IC), Which shows the most suitable design methods for low-voltage analog IC design in a standard CMOS process include techniques using bulk-driven MOS transistors, dynamic threshold MOS transistors and MOS transistors operating in weak or moderate inversion regions. Basic circuit building blocks like differential amplifiers or current mirrors designed using these approaches are able to operate with the power supply voltage of 600 mV or even lower, which is the key feature towards integrated systems for modern portable applications.

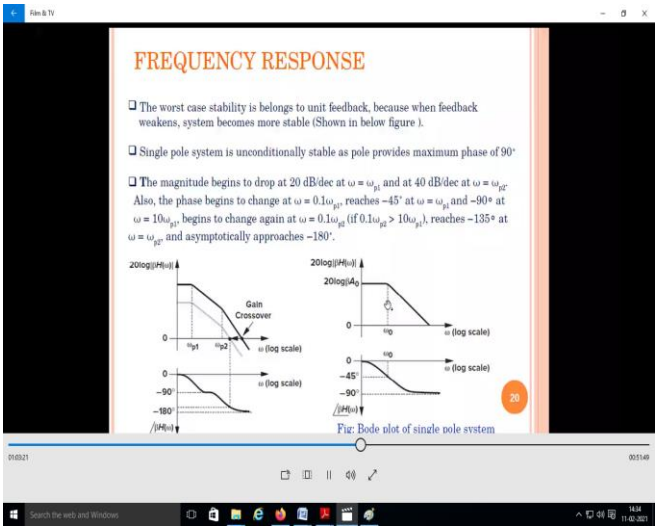


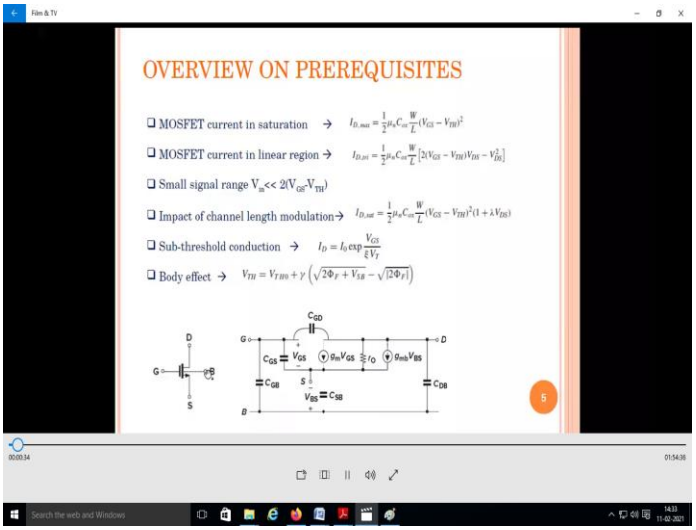


Day 1: 28th Dec 2020 [AN]

Topics : Design of Op-Amp, Frequency response & Stability analysis of Op-Amp.
Resource Person : Dr. K. Vasudeva Reddy, Senior Design Engineer, Mbit Wireless Pvt. Ltd, Chennai

The resource Person, **Dr. K. Vasudeva Reddy**, Senior Design Engineer, Mbit Wireless Pvt. Ltd, Chennai has discussed about future generation digital circuit cores that provide main circuit implementation approach for Integrated Circuit (IC) functions in Very Large Scale Integration (VLSI) circuits and systems. The discussion focused on the design of the op-amp using different compensation schemes and focused on the open-loop frequency response performance of the op-amp.

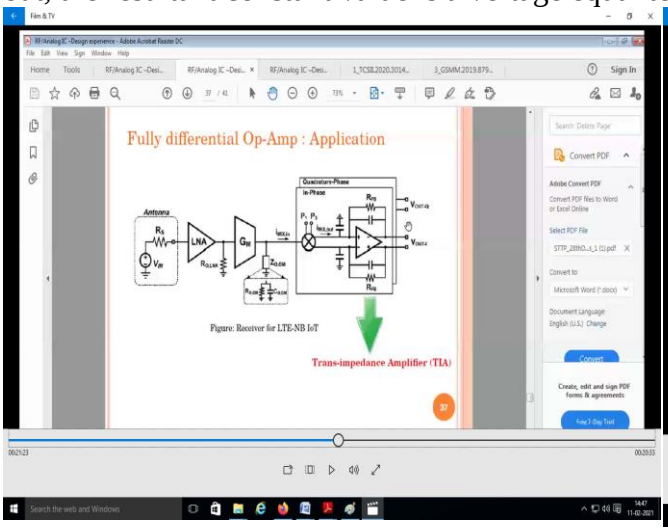


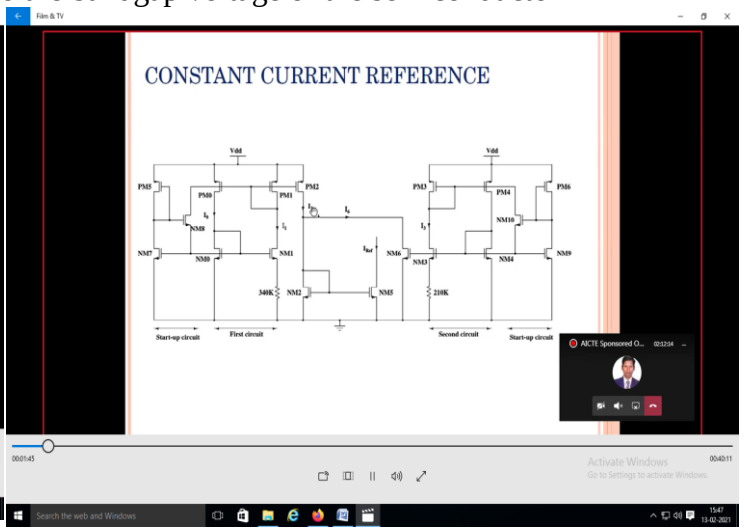


Day 2: 29th Dec 2020 [FN]

Topics : Current and Voltage reference, Band gap reference circuits
Resource Person : Dr. K. Vasudeva Reddy, Senior Design Engineer, Mbit Wireless Pvt. Ltd, Chennai

The resource Person, **Dr. K. Vasudeva Reddy**, started his lecture by giving a brief overview on previous lecture and started with Band gap voltage references which are indispensable in any analog/mixed-signal system. In his lecture he explained about systematic gm/ID-based procedure to design a CMOS band gap reference. The most common voltage reference circuit used in integrated circuits is the bandgap voltage reference. A band gap based reference uses analog circuits to add a multiple of the voltage difference between two bipolar junctions biased at different current densities to the voltage developed across a diode. The diode voltage has a negative temperature coefficient, and the junction voltage difference has a positive temperature coefficient. When added in the proportion required to make these coefficients cancel out, the resultant constant value is a voltage equal to the bandgap voltage of the semiconductor

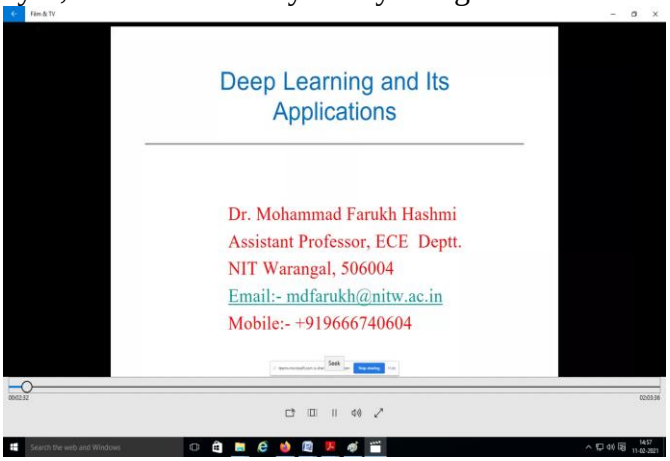


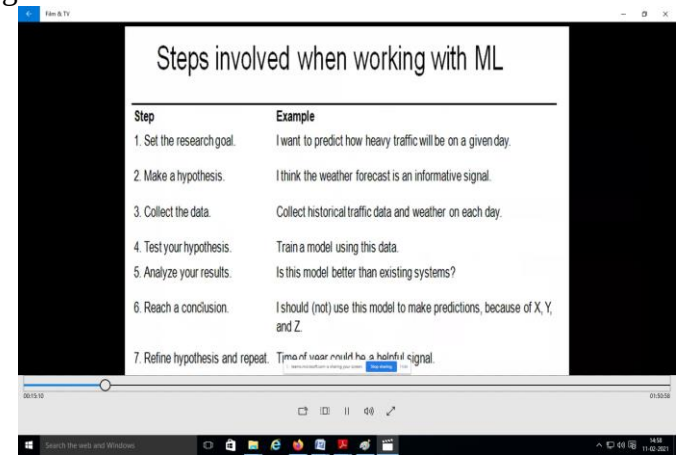


Day 2: 29th Dec 2020 [AN]

Topics : Deep Learning and its applications
Resource Person : Dr. Mohammad Farukh Hashmi, Assistant Professor, NITW, Warangal

The resource Person, **Dr. Mohammad Farukh Hashmi,** explored insights of Deep Learning, and Deep Learning continues to fascinate us with its endless possibilities such as fraud detection and pixel restoration and the applications of deep learning across industries, and highlighted as **Deep Learning** is a subfield of machine learning concerned with algorithms inspired by the structure and function of the brain called **artificial neural networks**. In deep learning, each level learns to transform its input data into a slightly more abstract and composite representation. In an image recognition application, the raw input may be a matrix of pixels; the first representational layer may abstract the pixels and encode edges; the second layer may compose and encode arrangements of edges; the third layer may encode a nose and eyes; and the fourth layer may recognize that the image contains a face.



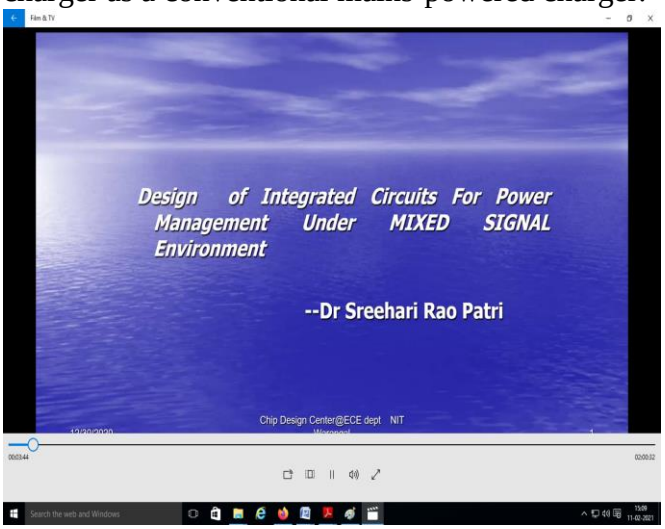


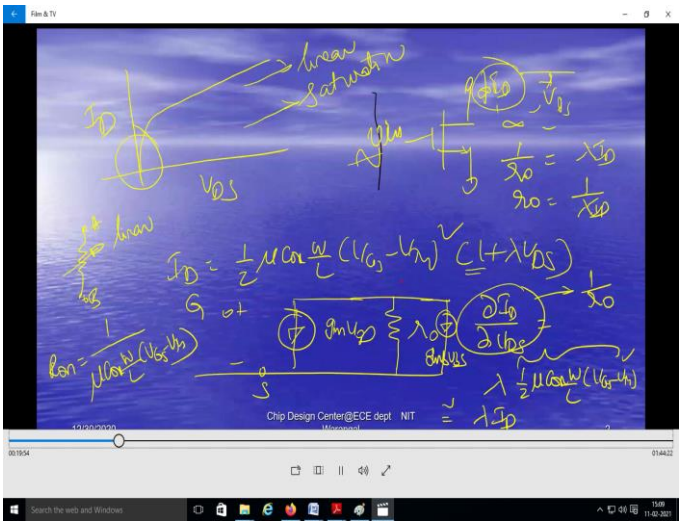
Day 3: 30th Dec 2020 [FN]

Topics : Challenges in Mixed Signal IC Design with power management Perspective and LDO

Resource Person : Dr. P Srihari Rao, Associate Professor, NITW, Warangal

The resource Person **Dr. P Srihari Rao**, started his lecture on Power Management challenges, which is one of the big concerns in IC design industry today. Power management chips are the key components in any device with a power supply, battery or power cord, which exist primarily to optimize power usage. In short, they serve as a bridge for electricity to flow through a system or device. Power-management functions must be complex enough to handle the increasing number of peripherals and processor cores populating today's mobile platforms. Power management must also deal with more complex charging scenarios, as today's users are as apt to charge their devices from sources like a PC USB port or car charger as a conventional mains-powered charger.



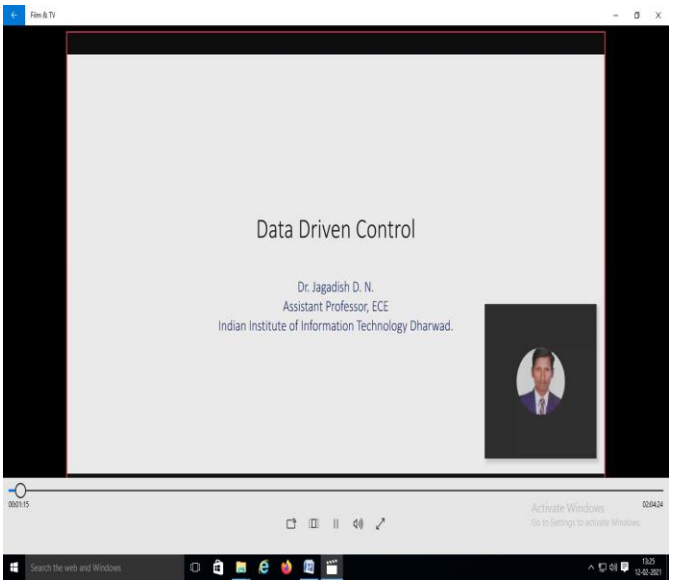


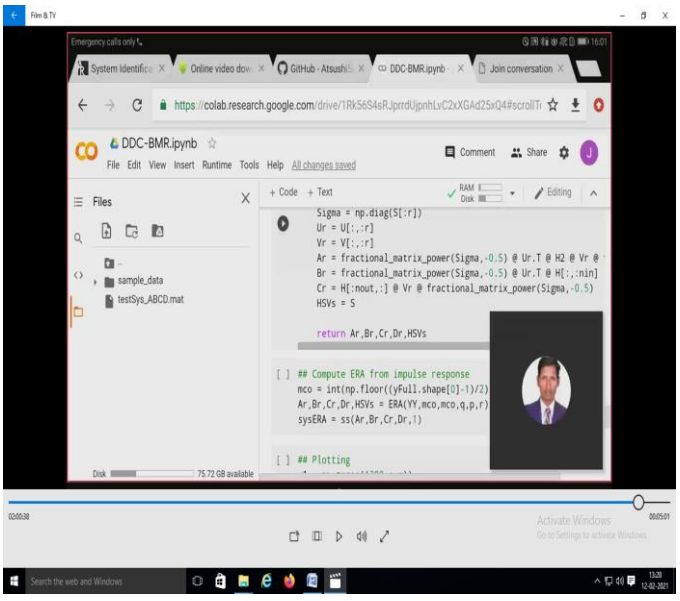
Day 3: 30th Dec 2020 [AN]

Topics : Data driven Control

Resource Person : Dr. Jagadish D. N., IIIT Dharwad

The Resource Person, **Dr. Jagadish D. N**., in his lecture described about DDC which means the control theory and method in which the controller is designed by directly using online or offline I/O data obtained from the controlled system or knowledge from data processing, instead of first modeling the controlled plant and then designing the controller using the process physical model obtained. Meanwhile, the stability, convergence, and robustness could be guaranteed by rigorous mathematical analysis under certain reasonable assumptions. Data driven learning systems imply that the system functions, such as modeling, decision, optimization, scheduling, monitoring and diagnosis, maintenance, are all implemented only by using the data or the knowledge from the data when the physical model is unavailable.



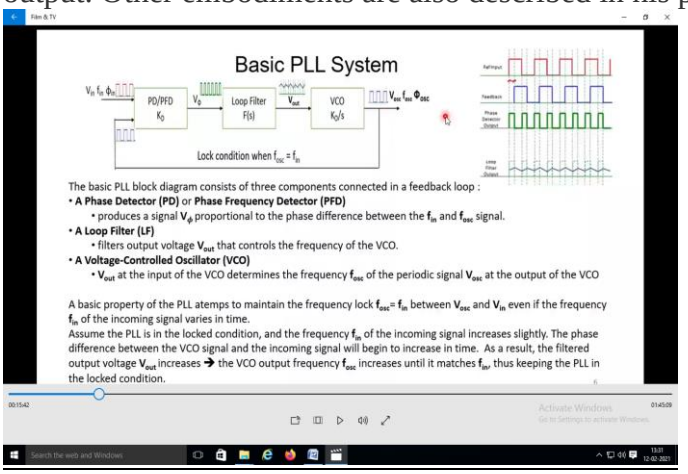


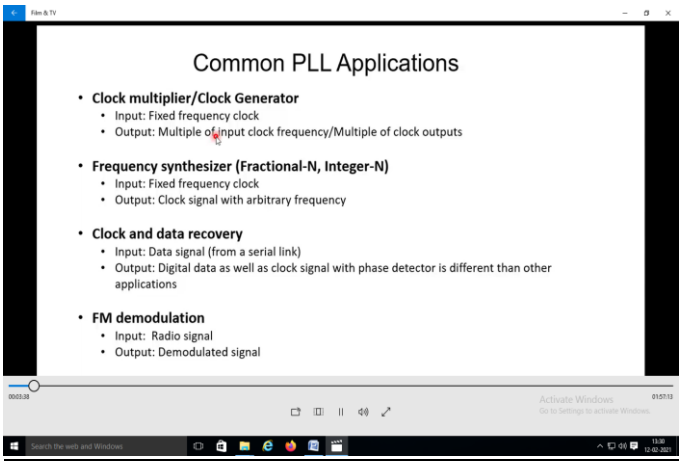
Day 4: 31st Dec 2020 [FN]

Topics **: PLL, Switched capacitor circuits**

Resource Person **: Dr. Krishna Reddy, Design Engineer, AMD India private Ltd, Hyderabad.**

The resource person **Dr. Krishna Reddy** in his presentation focused on how a filter couples an output of a phase detector to an input of a voltage controlled oscillator. The discussion about how the filter has a first capacitor and a switch capacitor resistor that is in series with the first capacitor, between the first capacitor and the output of the phase detector, and the switch capacitor resistor is to display a resistance that is obtained by switching back and forth a second capacitor to the first capacitor and to the phase detector output. Other embodiments are also described in his presentation



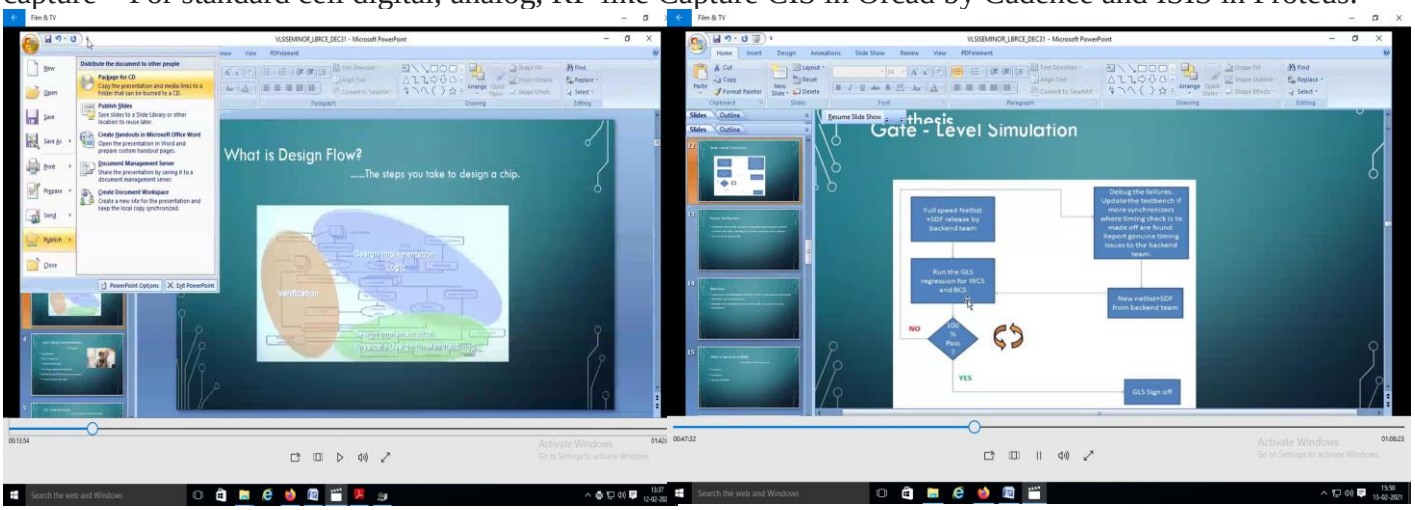


Day 4: 31st Dec 2020 [AN]

Topics **:** VLSI Industry (Overall introduction)
How Front End designer will help the VLSI Industry

Resource Person : Mr. N. Vijayakanth
Co-founder & CEO of VLSIMONKS, Bangalore
Mr. N. Srikanth, Technical Member Staff
SeviTech Systems Pvt. Ltd., Bangalore.

Mr. N. Vijayakanth started the discussion with VLSI began in the 1970s when MOS integrated circuit chips were widely adopted, enabling complex semiconductor and telecommunication technologies to be developed. The microprocessor and memory chips are VLSI devices. Before the introduction of VLSI technology, most ICs had a limited set of functions they could perform. Design Flow primarily remains characterized via several primary components; these include: High-level synthesis (additionally known as behavioral synthesis or algorithmic synthesis) – The high-level design description (e.g. in C/C++) is converted into RTL or the register transfer level, responsible for representing circuitry via the utilization of interactions between registers. Logic synthesis – The translation of RTL design description into a discrete netlist or representation of logic gates. Schematic capture – For standard cell digital, analog, RF-like Capture CIS in Orcad by Cadence and ISIS in Proteus.

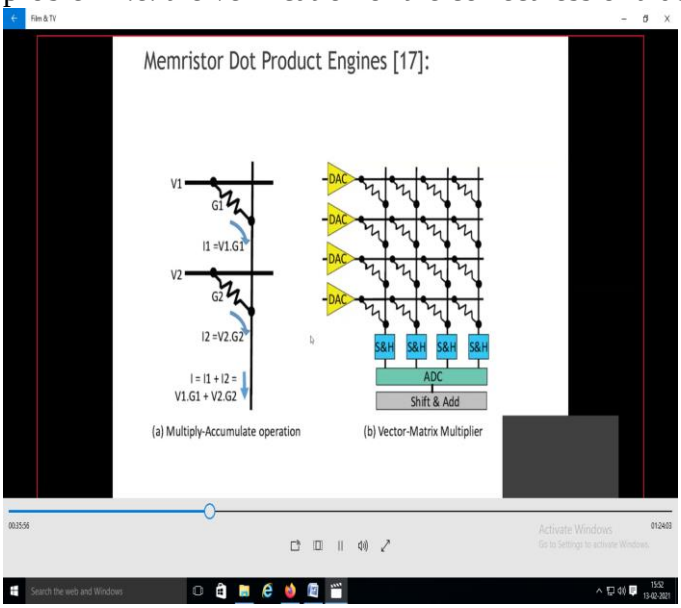


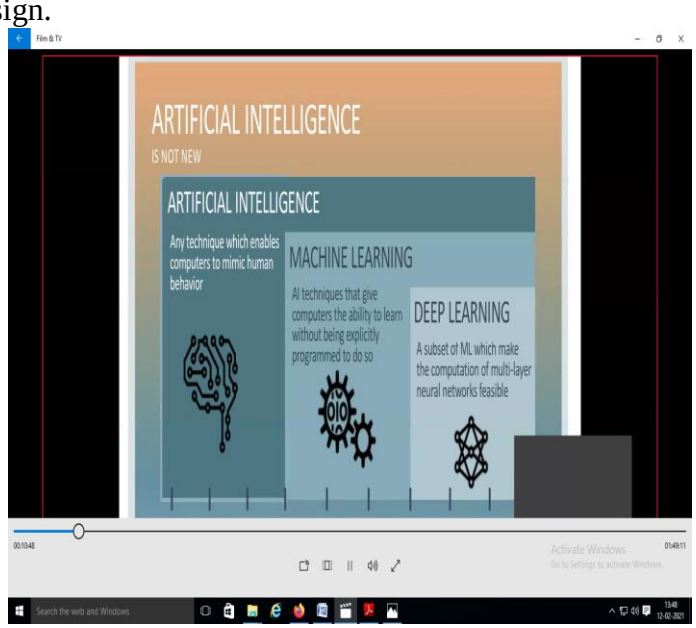
Day 5: 2nd Jan 2021[FN]

Topics : **VLSI architectures for AI Processors**

Resource Person : Dr. Shaik Rafi Ahamed, Professor, IITG, Guwahati.

The resource Person, **Dr. Shaik Rafi Ahamed**, in his lecture explained about the most of the prosperous applications of Artificial Intelligence (AI) to integrated circuit and printed circuit board design schematic appeared in the area of expert systems which work as design assistants .The expert systems technology is only one aspect of AI. VLSI design is a complex process. The complexity is multi-dimensional. Size and level of detail are two distinctive dimensions which include the hierarchical nature of the design process as well as of the self-design. AI languages lend themselves to solving problems of such complexity. These language features coupled with expert systems permit a significant first step to solving a very difficult problem i.e. the verification of the correctness of a design.



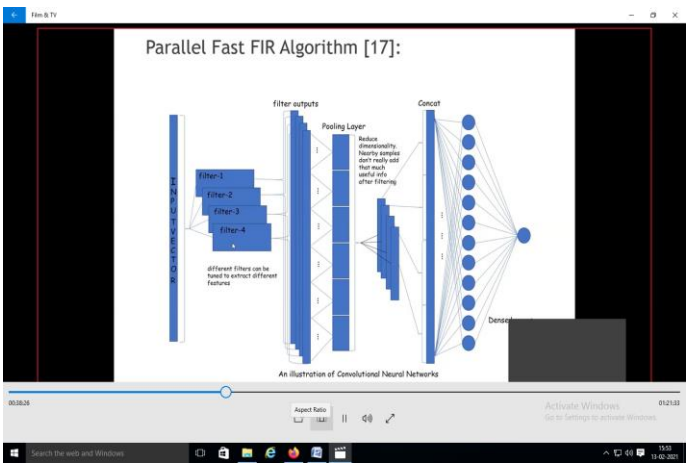


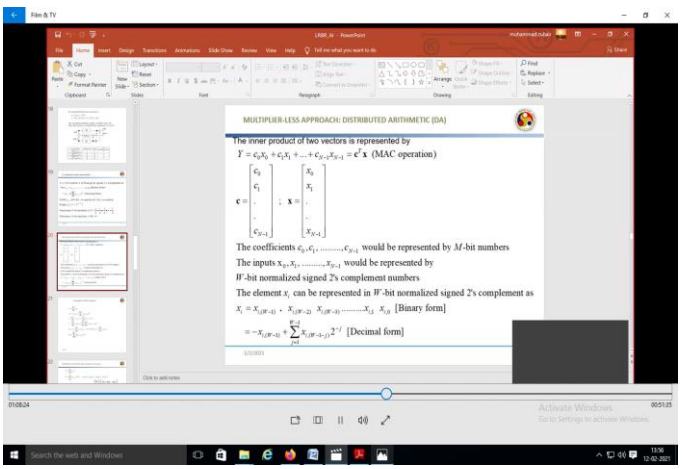
Day 5: 2nd Jan 2021[AN]

Topics : W**hat is the role of Physical Design in VLSI?**

Resource Person : Mr. N. Vijayakanth, Co-founder and CEO of VLSIMONKS, Bangalore

The resource Person **Mr. N. Vijayakanth**, given his lecture on the role of Physical Design in VLSI and describe about the task of VLSI physical design is to produce the layout of an integrated circuit which is one of the important steps in creating a VLSI circuit is its physical design. The input to the physical design step is a logical representation of the system under design. P**hysical design** is a step in the standard design cycle which follows after the circuit design. At this step, circuit representations of the components (devices and interconnects) of the design are converted into geometric representations of shapes which, when manufactured in the corresponding layers of materials, will ensure the required functioning of the components. This geometric representation is called integrated circuit layout.



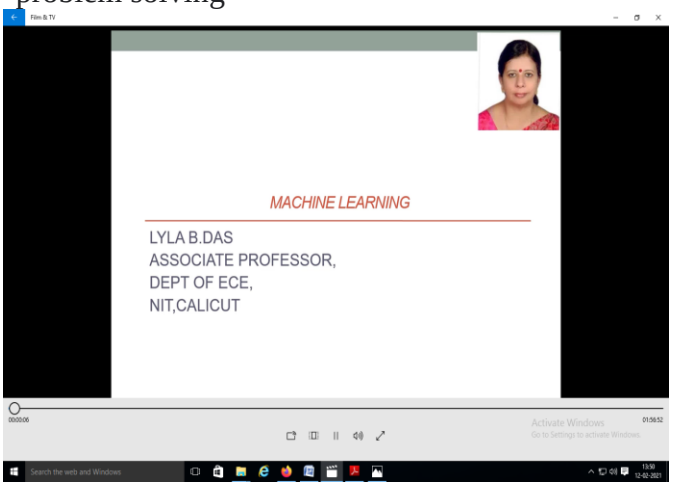


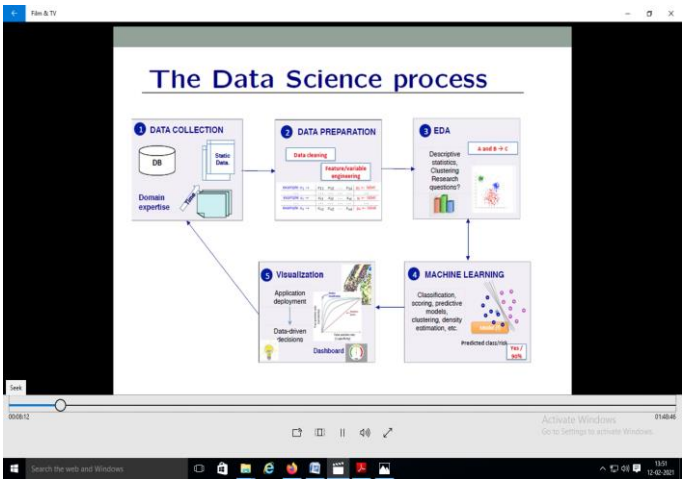
Day 6: 3rd Jan 2021[FN]

Topics : **AI and ML**

Resource Person : Ms. Lyla B. Das, Associate Professor, NIT Calicut, Calicut

The resource Person **Ms. Lyla B. Das** in his lecture described about AI & MI: **Artificial Intelligence** (**AI) and Machine Learning** (**ML**) are two very hot buzzwords right now, and often seem to be used interchangeably. The Machine Learning is a current application of **AI** based around the idea that we should really just be able to give machines access to data and let them learn for themselves. AI is intelligence demonstrated by machines. The distinction between the former and the latter categories is often revealed by the acronym chosen. 'Strong' AI is usually labelled as AGI (Artificial General Intelligence) while attempts to emulate 'natural' intelligence have been called ABI (Artificial Biological Intelligence). Leading AI textbooks define the field as the study of "intelligent agents": any device that perceives its environment and takes actions that maximize its chance of successfully achieving its goals. Colloquially, the term "artificial intelligence" is often used to describe machines (or computers) that mimic "cognitive" functions that humans associate with the human mind, such as "learning" and "problem solving



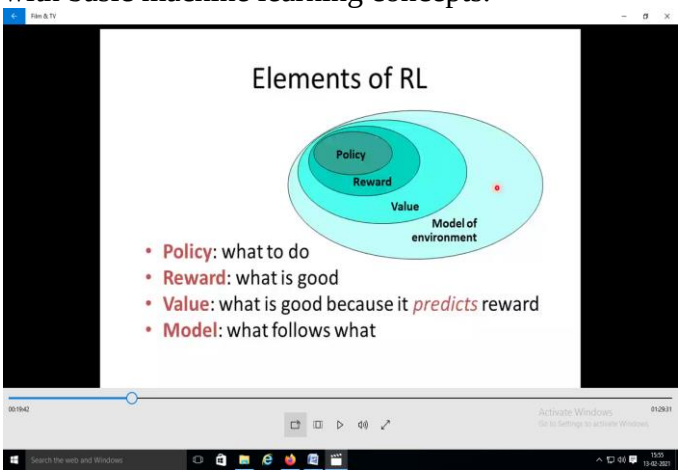


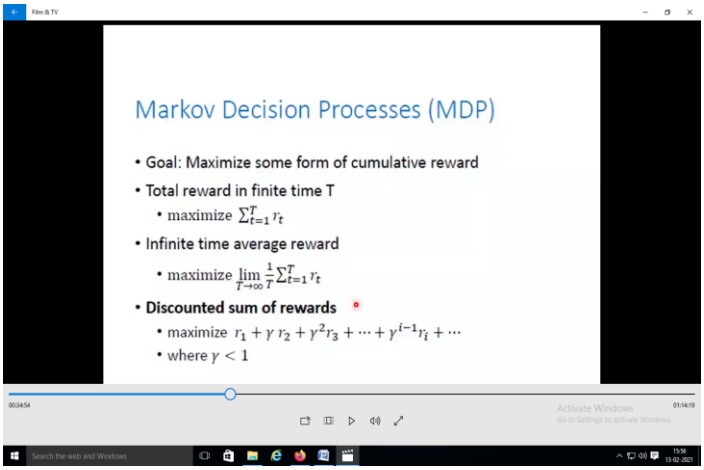
Day 6: 3rd Jan 2021[AN]

Topics : **RL and Deep Learning**

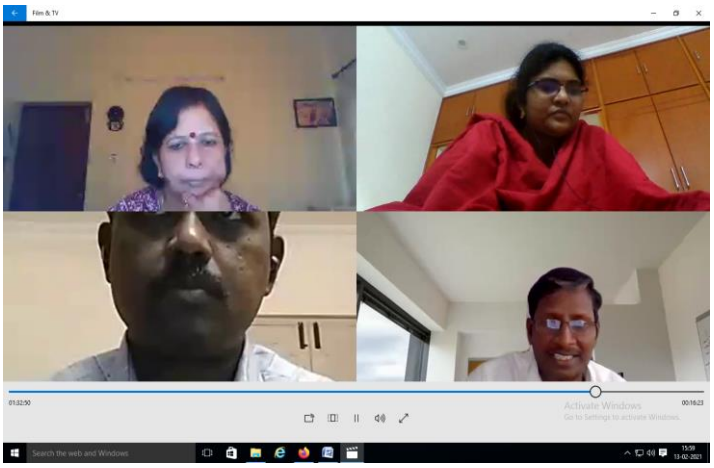
Resource Person : Ms. Lyla B. Das, Associate Professor, NIT Calicut, Calicut

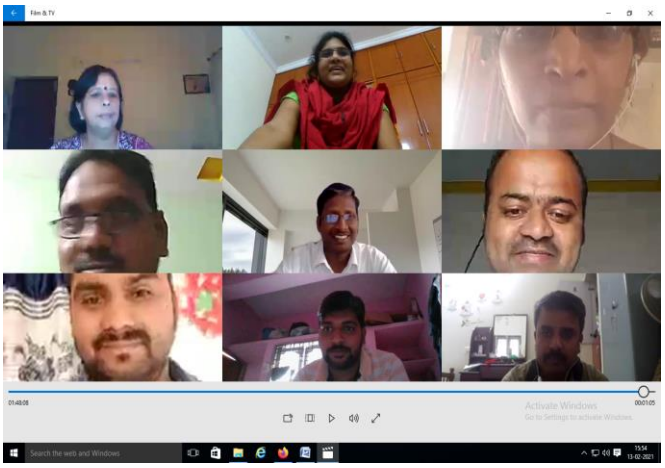
The resource Person **Ms. Lyla B. Das** in his lecture described about RL & Deep Learning:Deep reinforcement learning is the combination of reinforcement learning (RL) and deep learning. This field of research has been able to solve a wide range of complex decision-making tasks that were previously out of reach for a machine. Thus, deep RL opens up many new applications in domains such as healthcare, robotics, smart grids, finance, and many more. This manuscript provides an introduction to deep reinforcement learning models, algorithms and techniques. Particular focus is on the aspects related to generalization and how deep RL can be used for practical applications. We assume the reader is familiar with basic machine learning concepts.





Date: 03rd Jan 2021: Valedictory Session:





STTP Valedictory Session held on 03rd January 2021 at 3:45 PM by Coordinator of STTP **Dr. Srinivasulu Gundala,** Convener of STTP **Dr. Y. Amar Babu** along with Principal of LBRCE **Dr. K. Appa Rao,** chief guest of the programme **Ms. Lyla B. Das, Associate Professor, NIT Calicut, Calicut**, and Participants. Dr. K. Appa Rao in his valedictory addressing, conveyed his wishes to all the participants of STTP, congratulated the Program Convener Dr. Y. Amar Babu and Coordinator Dr. Srinivasulu Gundala for organizing the STTP in a successful manner. Further, he appreciated all the Teaching and Non-Teaching Staff Members of ECE Department for promoting such kind of development programme. He also motivated to keep learning new technologies coming in future for the career growth as well as organizational growth.

At the end of the valedictory session, vote of thanks was given by **Dr. Srinivasulu Gundala, Coordinator of the STTP** in which he has been paid his gratitude to AICTE for sponsoring the STTP program, resource persons for spending valuable time for our participants and sharing the knowledge and all the participants for attending this STTP.

Expressed the gratitude to the **LBRCE management**, Principal **Dr**. **K. Appa Rao,** Dean R & D **Dr. E. V. Krishna Rao** and team, Teaching and non-teaching staff members of ECE dept. and Microsoft Teams online software providers for extending support and for providing us with an environment to complete STTP program successfully.

Feedback from the Participants:

The feedback of the participants was very positive and motivational for the organizers. The participants felt very happy for conducting the STTP on latest trends in Industry. They said that, this program was very useful and helpful for them in their research, in turn guiding students in latest technologies. All the participants appreciated the sessions organized by the department of ECE and the arrangements made by the organizers.

The number of Online registrations by the Faculty members and Research scholars of AICTE approved institutions and were 79 for Series- 1, on an average 67 participants participated in online sessions, based on the eligibility criteria of the AICTE norms the e-certificates were issued to 46 participants.

10.01.2021

Coordinator
(Dr. Srinivasulu Gundala)

Convener
(Dr. Y. Amar Babu)